



## Switched capacitor DC-DC converter with switch conductance modulation and Pseudo-fixed frequency control

Larsen, Dennis Øland; Vinter, Martin; Jørgensen, Ivan Harald Holger

*Published in:*

43rd IEEE European Solid State Circuits Conference (ESSCIRC 2017)

*Link to article, DOI:*

[10.1109/ESSCIRC.2017.8094581](https://doi.org/10.1109/ESSCIRC.2017.8094581)

*Publication date:*

2017

*Document Version*

Peer reviewed version

[Link back to DTU Orbit](#)

*Citation (APA):*

Larsen, D. Ø., Vinter, M., & Jørgensen, I. H. H. (2017). Switched capacitor DC-DC converter with switch conductance modulation and Pseudo-fixed frequency control. In *43rd IEEE European Solid State Circuits Conference (ESSCIRC 2017)* IEEE. <https://doi.org/10.1109/ESSCIRC.2017.8094581>

---

### General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

# Switched Capacitor DC-DC Converter with Switch Conductance Modulation and Pseudo-Fixed Frequency Control

Dennis Øland Larsen<sup>\*†</sup>, Martin Vinter<sup>†</sup>, Ivan Jørgensen<sup>\*</sup>

<sup>\*</sup>Department of Electrical Engineering, Technical University of Denmark, Kongens Lyngby, Denmark

<sup>†</sup>R&D Hardware Platforms IC, GN Hearing A/S, Ballerup, Denmark

Email: deno@elektro.dtu.dk

**Abstract**—A switched capacitor dc-dc converter with frequency-planned control is presented. By splitting the output stage switches in eight segments the output voltage can be regulated with a combination of switching frequency and switch conductance. This allows for switching at predetermined frequencies, 31.25 kHz, 250 kHz, 500 kHz, and 1 MHz, while maintaining regulation of the output voltage. The controller is implemented in 180 CMOS with a 1/3 series-parallel output stage designed for 3.6–4.2 V input, 1.2 V output, and 1–40 mA load current. The proposed controller is compared with a co-integrated pulse skipping controller and yields a 84.8% reduction in worst-case low-load output ripple voltage and a 1.5% increase in peak efficiency reaching 92.5%, while also providing a predictable spectrum of the switching noise, reducing the risk of interfering with other sensitive circuits.

## I. INTRODUCTION

The increased integration of electronic systems has led to the development of portable battery-powered products that provide people with a broad range of benefits. A modern hearing aid is a good example of a heavily integrated device, which in a small form factor combines advanced audio processing from multiple microphones, an audio output stage, and Bluetooth communication for audio streaming, device configuration, and communication between two hearing aids. The many features result in substantial power consumption when compared with the available energy in the small battery.

In a small wearable device like a rechargeable hearing aid the noise generated by the power supplies is an issue. Both the microphone channels, class D amplifier, and the Bluetooth and telecoil radio systems are susceptible to noise in certain frequency bands, and they are all placed in close proximity to the power converters. Combined with the desire to use frequency modulation control to ensure a high power conversion efficiency makes the control of the power converters especially challenging.

Recent research in switched capacitor converters (SCCs) has mainly focused on fully integrated converters for microprocessors. Fully integrated power conversion is a necessity in e.g. point of load converters for dynamic voltage and frequency scaling on individual processor cores, and for reducing the number of power pads on high performance microprocessors. For a low power system like a hearing aid, where the typical supply current is in the order of 1 mA, loss in the power

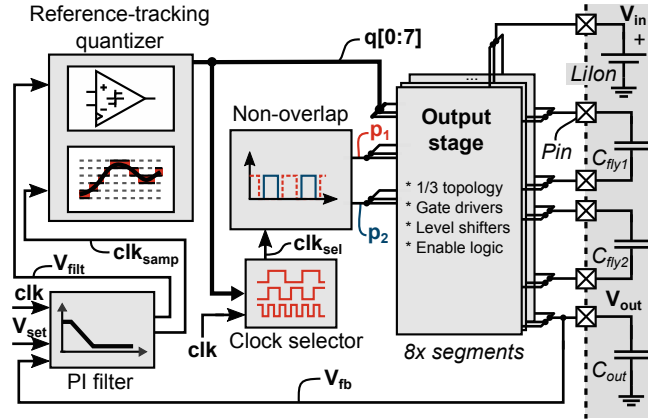


Fig. 1. The proposed converter consisting of a 1/3 output stage where each switch is split in eight segments, a switched capacitor PI filter, a single-comparator 9-level quantizer, and the clock selection logic. The output stage takes the switch conductance selection vector  $q[0:7]$  and the two non-overlapping clock signals  $p_1$  and  $p_2$  as inputs.

distribution network is small. Having the power converter integrated with the DSP is therefore not a necessity and having a dedicated power management IC (PMIC) allows for more flexibility in the choice of process technology when having to interface to Li-Ion battery voltage levels (3.0–4.2 V). The PMIC should be designed for high efficiency to give a long operating time between recharging the Li-ion battery and the power density should be high to keep the hearing aid small.

In this paper we present an SCC with frequency planned control that ensures that most of the switching energy is located at predetermined frequencies in contrast to most prior art [1], [2]. The use of external multi layer ceramic capacitors (MLCCs) results in a competitive power density and the proposed control results in a reduction in both output voltage ripple and the input peak currents when compared with a traditional pulse skipping control scheme. In Section II the design and modeling of a 1/3 topology SCC output stage is described and in Section III the proposed controller design is presented. In Section IV measurement results on a prototype IC in 180 nm CMOS are presented and in Section V the paper findings are summarized.

## II. SWITCHED-CAPACITOR OUTPUT STAGE DESIGN AND MODELING

The operation, modeling, and design of SCCs have been widely studied in the literature [3], and we will therefore focus on the specifics of the pseudo fixed frequency controller. An SCC consists of an output stage and a controller. The output stage used for evaluating the controller is a 1/3 series-parallel topology, such as the one reported in [4], and it consists of two flying capacitors and seven switches. Before defining the output stage operating points for the controller in Section II-B we need to understand the dynamics of the output stage.

### A. Output Stage Fundamentals

The output stage has two inputs (see Fig. 1): the selected clock signal  $clk\_sel$  (having a certain frequency  $F_{sw}$ ) and the number of selected switch segments in the output stage  $q[0:7]$  (leading to a certain switch conductance  $G_{sw}$ ). In this way both the switch conductance  $G_{sw} = 1/R_{sw}$  and output stage switching frequency  $F_{sw}$  can be controlled by having a proportional-integral (PI) controller slide between eight operating points. Each operating point is defined with a certain  $G_{sw}$  and  $F_{sw}$  value. We therefore need to establish the output stage dynamics at the eight operating points.

The output stage operates by periodically connecting the two flying capacitors in Fig. 1 in parallel with  $V_{out}$  or in series between  $V_{in}$  and  $V_{out}$ . The output voltage of an SCC can be expressed as a function of the equivalent converter output impedance  $R_{out}$ :

$$V_{out} = NV_{in} - R_{out}I_{load}. \quad (1)$$

This widely used model [5], reveals that  $R_{out}$  has to be controllable in order to maintain a desired  $V_{out}$  when both  $V_{in}$  and  $I_{load}$  are varying given that  $N = 1/3$  is fixed by the topology. The expressions for  $R_{out}$  in the two extremes, slow switching limit (SSL) and fast switching limit (FSL), for when the switching period is much greater or smaller than the time constant of  $C_{fly}$  and the switch resistance, shows how  $R_{out}$  depends on  $R_{sw}$  and  $F_{sw}$  [3]:

$$R_{SSL} = \frac{1}{4.5C_{fly}F_{sw}}, \quad R_{FSL} = \frac{14}{9}R_{sw} \approx 1.56R_{sw}. \quad (2)$$

Here  $R_{sw}$  is the resistance of each switch and  $C_{fly}$  is the capacitance of each flying capacitor.

The minimum equivalent output impedance  $R_{out,min}$  is achieved at the maximum  $F_{sw}$ .  $R_{out,min}$  is chosen based on the  $I_{load}$  specifications and the desired minimum  $V_{in}$  where the controller can still maintain  $V_{out}$  at the desired voltage. The controller presented here will be used with a multi topology gearbox output stage in the final implementation which adds another dimension in the decision of  $R_{out,min}$  of each topology. For the sake of comparing the proposed controller with the prior art the 1/3 output stage is designed to have  $R_{out,min} = 2\Omega$ , and the two flying capacitors are chosen to be  $C_{fly} = 185\text{ nF}$ , and  $C_{out} = 4.7\text{ nF}$ . With these values the equivalent output impedance  $G_{out} = 1/R_{out}$  can be evaluated as a function of  $G_{sw}$  and  $F_{sw}$ .

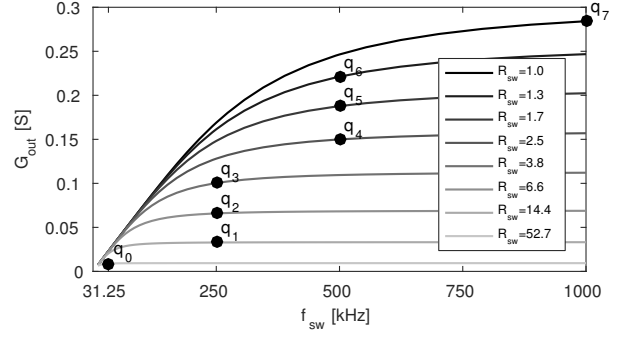


Fig. 2. The equivalent output conductance as a function of  $F_{sw}$  with one through eight switch segments engaged.

### B. State Space Model and Operating Points

An SCC is a switched linear system which makes it suited for modeling as a sampled data state space system [6]. By representing each of the two operating states as a linear system, the dynamics can be readily found. The model is used to design the eight operating points to be approximately equidistant in the  $G_{out}$  dimension. The maximum  $G_{sw}$  (the entire switch conductance) and maximum  $F_{sw}$  defines the top operating point  $q_7$  in Fig. 2. The frequency is increased when increasing  $G_{sw}$  only has little effect on the  $G_{out}$  which is the case when the converter is moved into SSL where the capacitors fully settle in each state.

## III. CONVERTER IMPLEMENTATION

The 1/3 output stage is fabricated together with the proposed controller and a pulse skipping controller in a 180 nm CMOS process (see Fig. 3). The main elements of the system are depicted in Fig. 1. To the right are the external flying capacitors and output filter capacitor, and next to that the output stage block comprising seven switches and necessary circuitry to interface between the 1.8V controller logic and the Li-Ion battery voltage domain. The output stage is operated in one of the eight operating points described above, or turned off if necessary. As there always is a base current consumption in the system the lowest  $G_{out}$  operating point can be designed to satisfy the lightest load scenario that the converter will be exposed to.

The clock selector block directly maps the number of enabled switch elements to a given clock frequency.  $F_{sw}$  of the different operating points can be extracted from Fig. 2<sup>1</sup>.

The switched capacitor PI controller filters the error signal  $V_{err} = V_{set} - V_{fb}$  ( $V_{fb}$  is  $V_{out}$  inside the chip before the bonding wire). It is clocked at 2 MHz and implemented using two OTAs and a network of switches and capacitors.

<sup>1</sup>In the implemented prototype ripple voltage is momentarily elevated when the controller switches between two clocks. E.g. when switching from the 250 kHz clock (having 2  $\mu$ s between clock transitions) to the 500 kHz clock (having 1  $\mu$ s between clock transitions) sometimes a single pulse of 3  $\mu$ s duration occurs (longer than for the two clock signals it is switching between) which causes the output voltage to drop. An updated clock selector correcting this problem is to be manufactured.

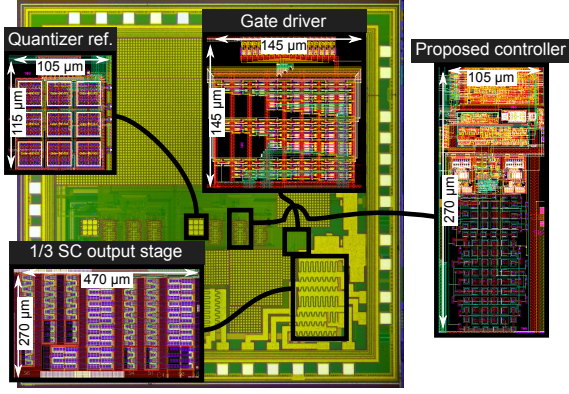


Fig. 3. Photograph of the prototype together with the layout of relevant blocks shown. The prototype was manufactured on a multi-project IC.

The filtered error signal  $V_{filt}$  is quantized by the reference tracking quantizer. The quantized  $V_{filt}$ ,  $q[0:7]$ , directly decides the output stage operating point. This causes the controller to continuously slide between the different operating points to minimize  $V_{err}$ . The controller operation can be understood by considering the situation where  $V_{out}$  drops due to an increase in  $I_{out}$ . This causes  $V_{err}$  to increase which will eventually cause  $V_{filt}$  to engage another level in the quantizer. This results in an increase in  $G_{out}$  which will cause more charge to be delivered to  $C_{out}$  effectively increasing  $V_{out}$  again.

The 9-level quantizer directly selects one of the eight operating points, or the state where all switch segments are turned off. It is implemented using a single low-power comparator having a moderate offset combined with a logic block (the reference tracker) that routes one of the eight reference voltage levels to the comparator. Only the level directly above and below the current quantization level is updated in each clock period to minimize power dissipation. By only using a single comparator, the offset of the comparator contributes the same to each quantization level and is therefore a constant common offset that is suppressed by the DC gain of the PI filter.

The output stage is implemented with 5 V transistors each designed to have equal conductance. The output stage requires three unique clock signals (two non overlapping clocks phases and one inverted phase for PMOS transistors). Multiplying this with eight switch segments results in 24 gate drivers. An automated buffer chain generator was implemented to optimize each gate driver to the specific gate capacitance to minimize the power dissipation.

#### IV. MEASUREMENT RESULTS

The proposed controller can be directly compared with the pulse skipping controller as both are implemented on the same chip. In the final application the PMIC would be flip-chip mounted but the prototype was wire bonded to a package. The resistance from a pad to package pin was measured to  $R_{BW} \approx 0.5 \Omega$ . The extra series resistance results in  $R_{out,min} = 3.7 \Omega$  instead of the expected  $2 \Omega$  without bonding wires. As the feedback loop for the controllers is

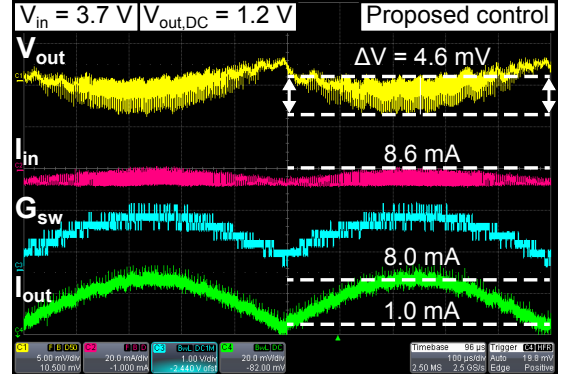


Fig. 4. Measured output voltage, input voltage, and the live switch conductance read-out, for a typical hearing aid load scenario and 3.7 V input.

closed inside the chip (notice  $V_{fb} \neq V_{out}$  in Fig. 1) the load regulation of the power converter is dominated by  $R_{BW}$ .

The operation of the proposed controller is demonstrated by loading it with a typical load scenario of a hearing aid: a base load of 1 mA DC plus a 7 mA rectified 1 kHz sinusoidal current waveform emulating a load from a full bridge audio output stage (i.e. the combined load goes from 1 mA to 8 mA)<sup>2</sup> with typical Li-ion battery voltage  $V_{in} = 3.7$  V. In Fig. 4  $I_{out}$  is shown together with a digital readout of  $G_{sw}$ , the input current  $I_{in}$ , and  $V_{out}$ . We observe that the controller chooses between the operating points in response to the  $I_{out}$  waveform. The peak  $I_{in}$  tracks the load current such that the power converter generates very little noise at low audio signal levels.

To investigate the transient load performance and to demonstrate how the controller helps minimize the  $V_{out}$  ripple and peak  $I_{in}$ , a step load from 1 mA to 25 mA is applied in Fig. 5. The measurements for the pulse skipping control in Fig. 5a shows constant  $V_{out}$  ripple and  $I_{in}$  peak values, and the varying  $F_{sw}$  is clearly observed. Notice that  $G_{sw}$  is not plotted for the pulse skipping controller as this type of controller always uses all the switch segments.

The  $V_{out}$  and  $I_{in}$  waveforms for the proposed controller in Fig. 5b clearly shows the benefits of modulating the switch conductance as both the output ripple and peak  $I_{in}$  are reduced. Especially the disturbances at the 1 mA load are reduced. The output voltage shows some undershoot, although the peak-peak value of  $V_{out}$  is still significantly lower than that of the pulse skipping controller. Notice that the  $G_{sw}$  values are mostly at very low values as the high input voltage level results in a high  $R_{out}$  being required to regulate  $V_{out}$ , referring to (1) (high  $R_{out}$  is achieved with low  $G_{sw}$ ).

In Fig. 6a and 6b the efficiency is plotted for various  $V_{in}$  and  $I_{out}$ . The proposed controller has lower efficiency at low load due to the higher power dissipation of the controller circuitry compared with the low power dissipation of the single comparator used in the pulse skipper. At higher currents the proposed controller has superior efficiency as it minimizes the

<sup>2</sup>At  $V_{in} = 3.7$  V we have to limit the load to 8 mA due to  $R_{BW}$  limiting  $R_{out,min}$  to  $3.7 \Omega$ . I.e.  $V_{out} = 3.7 \text{ V} / 3 - 3.7 \Omega \times 8 \text{ mA} = 1.2 \text{ V}$ . Without the  $R_{BW}$  we could have loaded it up to 16 mA at this specific  $V_{in}$ .

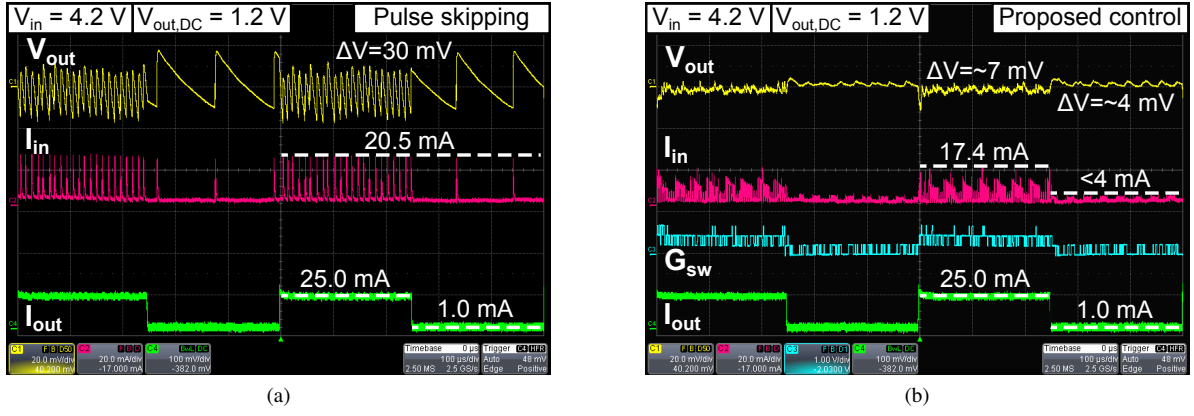


Fig. 5. Comparison of (a) pulse skipping and (b) the proposed controller for a load step.

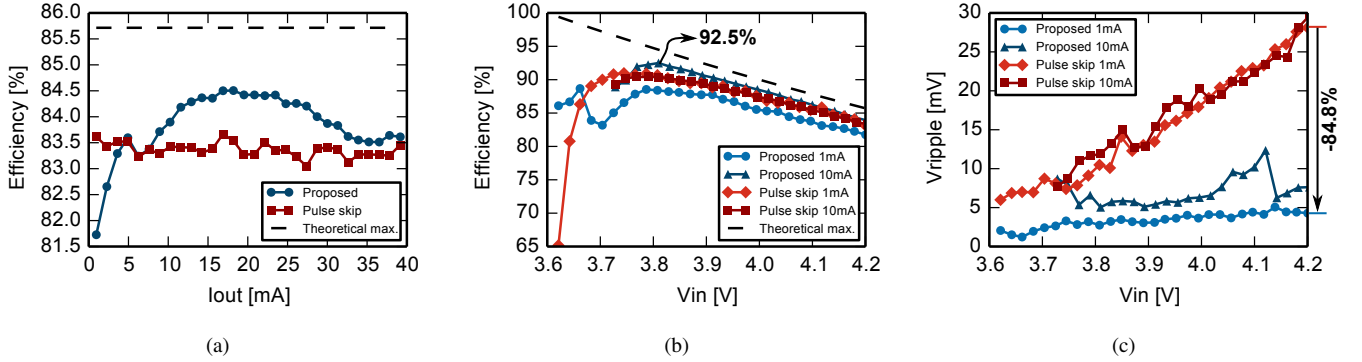


Fig. 6. Measured efficiency for (a) a load sweep with  $V_{in} = 4.2$  V and (b) an input voltage sweep, and (c) a the ripple voltage vs. input voltage.

gate losses by only charging a subset of the switch segments. The efficiency peaks at 92.45% for the proposed controller and at 90.96% for the pulse skipper. The proposed controller shows a 84.8% reduction in worst case ripple voltage in Fig. 6c.

## V. CONCLUSION

A frequency planned controller for switched capacitor dc-dc converters is presented and compared with a traditional pulse skipping controller. The controller uses a quantized version of the filtered error signal to configure the output stage to operate in one of eight operating points, each defined by a fixed switching frequency and switch conductance. The measurements show a 84.8% reduction in worst case output ripple voltage. At low load levels the proposed controller ensures minimal disturbances. The controller results in 1.5% increase in peak efficiency and higher efficiency at low battery voltage. Due to the higher power dissipation in the more complex controller, compared with pulse skipping, the efficiency is lower at low loads. In addition to this the controller ensures a predictable disturbance frequency spectrum.

## REFERENCES

[1] H. K. Kwan, D. C. W. Ng, and V. W. K. So, "Design and analysis of dual-mode digital-control step-Up switched-

capacitor power converter with pulse-skipping and numerically controlled oscillator-based frequency modulation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 11, pp. 2132–2140, 2013.

[2] T. Souvignat and B. Allard, "A Simple Approach to a Linear Control of Switched Capacitor DC-DC Converters in System-on-Chip," *Control and Modeling for Power Electronics (COMPEL)*, vol. 203, 2014.

[3] M. Seeman and S. Sanders, "Analysis and Optimization of Switched-Capacitor DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841–851, 2008.

[4] D. L. Ming, Y. H. Lee, and K. H. Chen, "A high efficiency adaptive frequency hopping controlled 1/3x step-down switch capacitor DC-DC converter with deep-green mode operation," *ISCAS 2012 - 2012 IEEE International Symposium on Circuits and Systems*, pp. 966–969, 2012.

[5] T. Van Breussegeem and M. Steyaert, *CMOS Integrated Capacitive DC-DC Converters*. New York, NY: Springer New York, 2013, vol. 3.

[6] T. Souvignat, B. Allard, and X. Lin-Shi, "Sampled-Data Modeling of Switched-Capacitor Voltage Regulator With Frequency-Modulation Control," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 4, pp. 957–966, Apr. 2015.